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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,062	11/14/2003	Shunpei Yamazaki	0756-7218	9062

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ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
LIU, BENJAMIN T	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/712,062	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Benjamin T. Liu	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/23/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 3-6 are rejected under 35 U.S.C 103(a) as being unpatentable over Miyawaki (5,717,473).

With regard to claim 1, figures 8A-8J of Miyawaki disclose a semiconductor device comprising: a channel region 3001 provided over a substrate 3 and between a source region and a drain region 1610; a gate electrode 1607 provided over the substrate 3 and provided adjacent to the channel region 3001 with a gate insulating film 1601 between the gate electrode 1607 and the channel region 3001; a first insulating film 1611 comprising silicon nitride ("SiN") provided over the channel region 3001 and the source region and the drain region 1610 and the gate electrode 1607 and the gate insulating film 1601; a second insulating film 1612 provided over the first insulating film 1611; a drain electrode 1613 connected with the drain region 1610 and provided over the second insulating film 1612; a source electrode 1613 connected with the source region 1610 and provided over the second insulating film 1612 a third insulating film provided 1616 over the drain electrode 1613 and the source electrode 1613 to provide a leveled surface ("flatten") over the drain electrode 1613 and the source electrode 1613;

a black matrix 1617 provided over the third insulating film 1616; a fourth insulating film 1618 provided over the black matrix 1617 to provide a third leveled surface ("flatten") over the black matrix 1617; and a pixel electrode 1619 connected with one of the drain electrode 1613 and the source electrode 1613 and provided over the fourth insulating film 1618.

Figures 8A-8J of Miyawaki does not disclose the first insulating film and comprising resin to provide a first leveled surface over said first insulating film, a third insulating film comprising resin, a fourth insulating film comprising resin.

However, figure 12 of Miyawaki discloses the insulating film 1915 comprising a resin ("resin"). Miyawaki also discloses an insulating layer deposited to flatten an etch back and the like. (Note line 35 col 6)

Therefore, it would have been obvious to one of ordinary skill in the art to form the device of figure 8A-8J of Miyawaki with the limitation of figure 12 of Miyawaki in order to stick two layers together. (Note lines 7-8 col 14 of Miyawaki)

With regard to claim 3, figures 8A-8J of Miyawaki disclose the limitation, wherein the semiconductor film has a thickness of 100 to 750 A ("100 to 700A"). (Note line 23 col 9)

With regard to claim 4, figures 8A-8J of Miyawaki disclose the limitation, wherein the semiconductor device is incorporated into one selected from the group consisting of a portable intelligent terminal, a head mounted display, a car navigational system, a mobile telephone, a portable video camera, and a projection display ("projection TV). (Note line 5 col 3)

With regard to claim 5, figures 8A-8J of Miyawaki disclose the limitation, wherein the semiconductor device is incorporated into a liquid crystal display. (Note title)

With regard to claim 6, figures 8A-8J of Miyawaki disclose the limitation, wherein the semiconductor device is incorporated into an electroluminescent display. (Note abstract)

Claim 2 is rejected under 35 U.S.C 103(a) as being unpatentable over Miyawaki (5,717,473) in view of Funai et al. (5,550,070).

With regard to claim 2, Miyawaki discloses all the subject matter claimed except for the limitation, wherein the channel region and the source region and the drain region are provided in a semiconductor film comprising a plurality of radial crystal grains of silicon.

However, figures 1-16 of Funai et al. disclose the limitation, wherein the channel region 118 and the source region 116 and the drain region 117 are provided in a semiconductor film 112 comprising a plurality of radial crystal grains of silicon 107.

Therefore, it would have been obvious to one of ordinary skill in the art to form the device of Miyawaki with the limitation of Funai et al. in order to control the crystal growth direction by selectively introducing the catalytic element. (Note lines 40-43 col 6 Funai et al.)

Claims 7, 9-13, and 15-18 are rejected under 35 U.S.C 103(a) as being unpatentable over Miyawaki (5,717,473) in view of Matsuo et al. (5,414,547).

With regard to claim 7, figures 8A-8J of Miyawaki disclose a semiconductor device comprising: a channel region 3001 provided over a substrate 3 and between a source region and a drain region 1610; a gate electrode 1607 provided over the substrate 3 and provided adjacent to the channel region 3001 with a gate insulating film 1601 between the gate electrode 1607 and the channel region 3001; a first insulating film 1611 comprising silicon nitride ("SiN") provided over the channel region 3001 and the source region and the drain region 1610 and the gate electrode 1607 and the gate insulating film 1601; a second insulating film 1612 provided over the first insulating film 1611; a drain electrode 1613 connected with the drain region 1610 and provided over the second insulating film 1612; a source electrode 1613 connected with the source region 1610 and provided over the second insulating film 1612 a third insulating film provided 1616 over the drain electrode 1613 and the source electrode 1613 to provide a leveled surface ("flatten") over the drain electrode 1613 and the source electrode 1613; a black matrix 1617 provided over the third insulating film 1616; a fourth insulating film 1618 provided over the black matrix 1617 to provide a third leveled surface ("flatten") over the black matrix 1617; and a pixel electrode 1619 connected with one of the drain electrode 1613 and the source electrode 1613 and provided over the fourth insulating film 1618.

Figures 8A-8J of Miyawaki does not disclose the first insulating film and comprising polyimide to provide a first leveled surface over said first insulating film, a third insulating film comprising polyimide, a fourth insulating film comprising polyimide.

However, figure 9 of Matsuo et al. discloses the insulating film 215 comprising a polyimide ("polyimide") to provide a leveled ("flatten") surface over the insulating film 215. (Note lines 1-15 col 21)

Therefore, it would have been obvious to one of ordinary skill in the art to form the device of figure 8A-8J of Miyawaki with the limitation of figure 9 of Matsuo in order to flatten the surface of the insulating film for the purpose of further improving the orienting characteristics of the liquid crystal. (Note lines 10-17 col 21 of Matsuo)

With regard to claim 9, figures 8A-8J of Miyawaki disclose the limitation, wherein the semiconductor film has a thickness of 100 to 750 A ("100 to 700A"). (Note line 23 col 9)

With regard to claim 10, figures 8A-8J of Miyawaki disclose the limitation, wherein the semiconductor device is incorporated into one selected from the group consisting of a portable intelligent terminal, a head mounted display, a car navigational system, a mobile telephone, a portable video camera, and a projection display ("projection TV). (Note line 5 col 3)

With regard to claim 11, figures 8A-8J of Miyawaki disclose the limitation, wherein the semiconductor device is incorporated into a liquid crystal display. (Note title)

With regard to claim 12, figures 8A-8J of Miyawaki disclose the limitation, wherein the semiconductor device is incorporated into an electroluminescent display. (Note abstract)

With regard to claim 13, figures 8A-8J of Miyawaki disclose a semiconductor device comprising: a channel region 3001 provided over a substrate 3 and between a source region and a drain region 1610; a gate electrode 1607 provided over the substrate 3 and provided adjacent to the channel region 3001 with a gate insulating film 1601 between the gate electrode 1607 and the channel region 3001; a first insulating film 1611 comprising silicon nitride ("SiN") provided over the channel region 3001 and the source region and the drain region 1610 and the gate electrode 1607 and the gate insulating film 1601; a second insulating film 1612 provided over the first insulating film 1611; a drain electrode 1613 connected with the drain region 1610 and provided over the second insulating film 1612; a source electrode 1613 connected with the source region 1610 and provided over the second insulating film 1612 a third insulating film provided 1616 over the drain electrode 1613 and the source electrode 1613 to provide a leveled surface ("flatten") over the drain electrode 1613 and the source electrode 1613; a black matrix 1617 provided over the third insulating film 1616; a fourth insulating film 1618 provided over the black matrix 1617 to provide a third leveled surface ("flatten") over the black matrix 1617; and a pixel electrode 1619 connected with one of the drain electrode 1613 and the source electrode 1613 and provided over the fourth insulating film 1618.

Figures 8A-8J of Miyawaki does not disclose the first insulating film and comprising resin to provide a first leveled surface over said first insulating film, a third insulating film comprising resin, a fourth insulating film comprising resin.

However, figure 12 of Miyawaki discloses the insulating film 1915 comprising a resin ("resin"). Miyawaki also discloses an insulating layer deposited to flatten an etch back and the like. (Note line 35 col 6)

Therefore, it would have been obvious to one of ordinary skill in the art to form the device of figure 8A-8J of Miyawaki with the limitation of figure 12 of Miyawaki in order to stick two layers together. (Note lines 7-8 col 14 of Miyawaki)

Miyawaki does not discloses the limitation, wherein at least a part of the black matrix is in contact with at least a part of the one of the drain electrode and the source electrode.

However, figure 9 of Matsuo discloses the limitation, wherein at least a part of the black matrix 216ba is in contact (electrically connected to pixel electrode 206 which is electrically connected to drain 207) with at least a part of the one of the drain electrode 207 and the source electrode. (Note abstract)

Therefore, it would have been obvious to one of ordinary skill in the art to form the device of Miyawaki with the limitation of Matsuo in order to obtain excellent display qualities by applying the same potential to the pixel electrode and black matrix and not disorientating the state of the liquid crystal. (Note lines 7-15 col 13 Matsuo et al.)

With regard to claim 15, figures 8A-8J of Miyawaki disclose the limitation, wherein the semiconductor film has a thickness of 100 to 750 A ("100 to 700A"). (Note line 23 col 9)

With regard to claim 16, figures 8A-8J of Miyawaki disclose the limitation, wherein the semiconductor device is incorporated into one selected from the group

consisting of a portable intelligent terminal, a head mounted display, a car navigational system, a mobile telephone, a portable video camera, and a projection display ("projection TV). (Note line 5 col 3)

With regard to claim 17, figures 8A-8J of Miyawaki disclose the limitation, wherein the semiconductor device is incorporated into a liquid crystal display. (Note title)

With regard to claim 18, figures 8A-8J of Miyawaki disclose the limitation, wherein the semiconductor device is incorporated into an electroluminescent display. (Note abstract)

Claims 8 and 14 are rejected under 35 U.S.C 103(a) as being unpatentable over Miyawaki (5,717,473) in view of Matsuo et al. (5,414,547) and further in view of Funai et al. (5,550,070).

With regard to claims 8 and 14, Miyawaki and Matsuo et al. discloses all the subject matter claimed except for the limitation, wherein the channel region and the source region and the drain region are provided in a semiconductor film comprising a plurality of radial crystal grains of silicon.

However, figures 1-16 of Funai et al. disclose the limitation, wherein the channel region 118 and the source region 116 and the drain region 117 are provided in a semiconductor film 112 comprising a plurality of radial crystal grains of silicon 107.

Therefore, it would have been obvious to one of ordinary skill in the art to form the device of Miyawaki and Matsuo et al. with the limitation of Funai et al. in order to

control the crystal growth direction by selectively introducing the catalytic element. (Note lines 40-43 col 6 Funai et al.)

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin T. Liu whose telephone number is (571) 272-6009. The examiner can normally be reached on Mon-Fri 9:30 AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached on 571 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BTL
4/9/2007